CLAIM AMENDMENTS

1. (Currently Amended) A semiconductor device comprising:

a first chip having an electrically rewritable nonvolatile memory;

a second chip including a memory having a redundant circuit and a circuit for memory test including a nonvolatile memory, said nonvolatile memory of said second chip storing

a test program for detecting whether there is a faulty portion in said memory of said second chip

a repair analysis program for identifying the faulty portion when the test program detects that there is a faulty portion in said memory of said second chip, and determining a portion in said redundant circuit that is to be utilized in place of the faulty portion, and

a software repair program for writing information required for utilizing the portion determined in said redundant circuit in place of the faulty portion identified by the repair analysis program in said nonvolatile memory of said first chip; and

a substrate on which said first chip and said second chip are ~~mounted~~ stacked, wherein information required for utilizing said redundant circuit in place of a faulty portion in said memory of said second chip is stored in said nonvolatile memory of said first chip, and said redundant circuit is utilized in place of the faulty portion in said memory of said second chip based on the information stored in said nonvolatile memory of said first chip.

Claim 2 (Cancelled)

3. (Previously Presented) The semiconductor device according to claim 1, wherein said nonvolatile memory in said circuit for memory test is rewritable.

4. (Previously Presented) A semiconductor device comprising:

a first chip having an electrically rewritable nonvolatile memory;

a second chip including a memory having a redundant circuit;

a third chip including a circuit for memory test having a nonvolatile memory, wherein said nonvolatile memory on said third chip stores

a test program for detecting whether there is a faulty portion in said memory of said second chip,

a repair analysis program for identifying the faulty portion when the test program detects that there is a faulty portion in said memory of said second chip, and determining a portion in said redundant circuit that is to be utilized in place of the faulty portion, and

a software repair program for writing information required for utilizing the portion determined in said redundant circuit in place of the faulty portion identified by the repair analysis program in said nonvolatile memory of said first chip; and

a substrate on which said first chip, said second chip, and said third chip are mounted, wherein information required for utilizing said redundant circuit in place of a faulty portion in said memory of said second chip is stored in said nonvolatile memory of said first chip, and said redundant circuit is utilized in place of the faulty portion in said memory of said second chip based on the information stored in said nonvolatile memory of said first chip.

5. (Original) The semiconductor device according to claim 4, wherein said nonvolatile memory in said circuit for memory test is rewritable.

Claim 6 (Cancelled).

7. (Previously Presented) The semiconductor device according to claim 4, wherein said first chip, said second chip, and said third chip are stacked on said substrate.

8. (Previously Presented) A semiconductor device comprising:

a first chip having an electrically rewritable nonvolatile memory;

a second chip including a memory comprising a circuit for memory test having a nonvolatile memory, wherein said nonvolatile memory of said second chip stores

a test program for detecting whether there is a faulty portion in said memory of said second chip,

a repair analysis program for identifying the faulty portion when the test program detects that there is a faulty portion in said memory of said second chip, and determining a position of a portion in said redundant circuit that is to be utilized in place of the faulty portion, and

a software repair program for writing information required for utilizing the portion determined in said redundant circuit in place of the faulty portion identified by the repair analysis program in said nonvolatile memory of said first chip;

a third chip having a redundant circuit; and

a substrate on which said first chip, said second chip, and said third chip are mounted, wherein information required for utilizing said redundant circuit of said third chip in place of a faulty portion in said memory of said second chip is stored in said nonvolatile memory of said first chip, and said redundant circuit of said third chip is utilized in place of the faulty portion in said memory of said second chip based on the information stored in said nonvolatile memory of said first chip.

Claim 9 (Cancelled)

10. (Previously Presented) The semiconductor device according to claim 8, wherein said nonvolatile memory in said circuit for memory test is rewritable.

11. (Previously Presented) A semiconductor device comprising:

a first chip having an electrically rewritable nonvolatile memory;

a second chip including a memory;

a third chip having a redundant circuit;

a fourth chip including a circuit for memory test having a nonvolatile memory, wherein said nonvolatile memory of said fourth chip stores,

a test program for detecting whether there is a faulty portion in said memory on said second chip,

a repair analysis program for identifying the faulty portion when the test program detects that there is a faulty portion in said memory of said second chip, and determining a position of a portion in said redundant circuit that is to be utilized in place of the faulty portion, and

a software repair program for writing information required for utilizing the portion determined in said redundant circuit in place of the faulty portion identified by the repair analysis program in said nonvolatile memory of said first chip; and

a substrate on which said first chip, said second chip, said third chip and said fourth chip are mounted, wherein information required for utilizing said redundant circuit of said third chip in place of a faulty portion in said memory of said second chip is stored in said nonvolatile memory of said first chip, and said redundant circuit of said third chip is utilized in place of the faulty portion in said memory of said second chip based on the information stored in said nonvolatile memory of said first chip.

12. (Original) The semiconductor device according to claim 11, wherein said nonvolatile memory in said circuit for memory test is rewritable.

13. (Previously Presented) The semiconductor device according to claim 8, wherein said first chip, said second chip, and said third chip are stacked on said substrate.

14. (Previously Presented) The semiconductor device according to claim 11, wherein said first chip, said second chip, said third chip, and said fourth chip are stacked on said substrate.